	L #	Hits	Search Text	DBs
1	L1	28267	stack near10 (frame area region space)	USPAT; US-PGPUB
2	L2	285	(bit field tag flag cod$3 encod$3) near10 (sav$3 stor$3) near15 1	USPAT; US-PGPUB
3	L3	12095	stack near10 (frame area region space)	EPO; JPO; DERWENT; IBM_TDB
4	L4	74	(bit field tag flag cod$3 encod$3) near10 (sav$3 stor$3) near15 3	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 2003288129 A	☐	MEMORY MANAGEMENT METHOD, MEMORY DEVICE, COMPUTER SYSTEM, COMPILER AND PROGRAM	
2	JP 2002253821 A	☐	GAME MACHINE	
3	JP 2002041326 A	☐	CENTRAL PROCESSING UNIT TO FACILITATE TEST AND DEBUGGING OF PROGRAM	
4	JP 2001353267 A	☐	GAME MACHINE	
5	JP 2002253821 A	☐	GAME MACHINE	
6	JP 2002041326 A	☐	CENTRAL PROCESSING UNIT TO FACILITATE TEST AND DEBUGGING OF PROGRAM	
7	JP 2001353267 A	☐	GAME MACHINE	
8	JP 2002052445 A	☐	MANUFACTURE OF INTEGRATED CIRCUIT ELEMENT	
9	JP 2002022242 A	☐	METHOD AND DEVICE FOR COMPILATION AND METHOD AND DEVICE FOR STACK TRACING	
10	JP 11085531 A	☐	LANGUAGE PROCESSOR AND STORAGE MEDIUM RECORDING PROGRAM REALIZING LANGUAGE PROCESSOR	
11	JP 10083305 A	☐	DATA PROCESSING SYSTEM WITH SELF-MATCHING STACK POINTER AND ITS METHOD	
12	JP 09231133 A	☐	CACHE MEMORY DEVICE	
13	JP 07160497 A	☐	MICROCOMPUTER	
14	JP 06290053 A	☐	CHARACTER-STRING CONSTANT LEXICAL ANALYZING SYSTEM	
15	JP 06152692 A	☐	CODING PROCESSING UNIT	
16	JP 05181712 A	☐	STACK HISTORY FORMING SYSTEM	
17	JP 05006281 A	☐	INFORMATION PROCESSOR	
18	JP 04334182 A	☐	PICTURE INPUT DEVICE	
19	JP 04040530 A	☐	REAL TIME PROCESSOR	
20	JP 03218529 A	☐	HIGH SPEED INTERRUPTION PROCESSOR	

	Document ID	U	Title	Current OR
21	JP 03211 687 A	☐	DATA TRANSFER CIRCUIT	
22	JP 03204 036 A	☐	COMPUTER WITH DYNAMIC RESTART MECHANISM AFTER INTERRUPTION PROCESSING	
23	JP 03075 940 A	☐	MULTITASK CONTROLLER	
24	JP 02217 947 A	☐	DATA PROCESSOR	
25	JP 02156 342 A	☐	PROGRAM DEBUGGING SYSTEM	
26	JP 02141 842 A	☐	MEMORY AREA REUSE PROCESSING SYSTEM	
27	JP 02077 841 A	☐	BACKTRACKING PROCESSING SYSTEM WITH LOGIC TYPE LANGUAGE	
28	JP 01112 339 A	☐	CODE MANAGING SYSTEM	
29	JP 01111 239 A	☐	ERROR DISPLAY SYSTEM	
30	JP 01041 934 A	☐	METHOD FOR PROCESSING STACK OF PROLOG MACHINE	
31	JP 63273 946 A	☐	DATA LOADING PROCESSOR	
32	JP 63255 704 A	☐	ARITHMETIC SYSTEM FOR SEQUENCER	
33	JP 63047 843 A	☐	INTERRUPTING SYSTEM FOR PROCESSING IN EXECUTION	
34	JP 62140 136 A	☐	DATA MEMORY DEVICE	
35	JP 62069 332 A	☐	STORING SYSTEM FOR HISTORY INFORMATION	
36	JP 61248 152 A	☐	PROCEDURE CHANGE CONTROLLING SYSTEM	
37	JP 61235 928 A	☐	KEY INPUTTING SYSTEM	
38	JP 61216 012 A	☐	PROCESSING SYSTEM FOR HIT OF POWER SUPPLY	
39	JP 61213 902 A	☐	NC DEVICE WITH AUTOMATIC THREE-DIMENSIONAL PROGRAMMING FUNCTION	
40	JP 61210 480 A	☐	FORMATION DATA MEMORY AND PROCESSING SYSTEM IN CAD/CAM SYSTEM	
41	JP 61136 128 A	☐	CONTROL PROCESSING SYSTEM CAPABLE OF REENTRANT OF PROGRAM	
42	JP 61131 130 A	☐	REGISTER SAVING METHOD	
43	JP 61029 943 A	☐	STACK CONTROL SYSTEM	

	Document ID	U	Title	Current OR
44	JP 60105 062 A	☐	STACK CONTROL METHOD	
45	JP 59165 145 A	☐	POINTER	
46	JP 59117 622 A	☐	TEXT INPUT CONTROLLING SYSTEM	
47	JP 57174 743 A	☐	INTERRUPTION PROCESSING CIRCUIT	
48	JP 57034 250 A	☐	PROGRAM CONTROLLING SYSTEM	
49	JP 56094 405 A	☐	SEQUENCE CONTROLLER	
50	JP 54074 649 A	☐	STACK CONTROL MECHANISM	
51	EP 80248 1 A1	☐	A data processing system having a self-aligning stack pointer and method therefor	
52	US 20030 13584 7 A	☐	Instrumented process reverting method in PC, cell phone, involves determining storage location of return pointer in call stack of process, and changing its value from instrumented code space to uninstrumented code space.	
53	US 20030 00738 4 A	☐	Non-volatile semiconductor memory e.g. EEPROM comprises stacked field effect transistors storing data of multibits and address space allocated in fixed position	
54	JP 20002 22242 A	☐	Compilation of Java program in network computing, involves storing address of execution code which changes stack pointer and information about size of stack frame after change, in memory	
55	US 60386 11 A	☐	API method for user-to-network interface signaling in ATM networks provides intelligent and flexible programming interface enabling higher layer software to set up and tear down ATM connections more efficiently	
56	US 59566 29 A	☐	Transmitter selection apparatus for mobile transmission within service area for vehicle	
57	US 59095 79 A	☐	Live pointer location encoding method in program data stack frame for computer system	
58	RD 41708 1 A	☐	Calling 64-bit functions from 32-bit functions - involves converting 32-bit registers to 64-bit, and changing processor mode of operation from 32-bit to 64-bit	
59	JP 10340 228 A	☐	Cache control system for microprocessor - prohibits replacement of stack area with respect to corresponding tag	
60	JP 10312 293 A	☐	Program development assistance apparatus - has conversion unit which converts read code into certain format which is then stored in stack area of memory, when converted format of each block is not matched with predefined information	
61	US 58325 26 A	☐	Tagging method for random access storage device - involves determining presence and amount of storage stack space in locally last storage sub-area, based on which end of file tagging code is recorded in that space	
62	KR 93088 83 B	☐	Stack capacitor mfr. - comprises patterning three layers of oxide, nitride and oxide and forming poly:silicon storage nodes	
63	KR 93007 17 B	☐	DRAM with stacked capacitor - includes V=shaped active region with bit line contact at vertex and storage node contacts at branch ends for honeycomb structure NoAbstract	

	Document ID	U	Title	Current OR
64	EP 492970 A	☐	Extending computer architecture from thirty-two to sixty-four bits - reviewing indication designating word size in registers each time restore operation occurs to determine size of word in procedure being restored	
65	JP 04161191 A	☐	Appts. to control speed of sewing machine drive motor - has RAM to store data for control mode of motor, speed setting, stitch number, embroidery data, etc., read from floppy disc	
66	US 5034886 A	☐	Computer system for reducing number of dedicated registers - using memory stock and sharing of address and general purpose registers wholly or partly composed of wide use register	
67	EP 437235 A	☐	Stacking system of single chip microcomputer - has stack area addressable to store 12 bit or 4 bit words changing assignment of data to RAM address according to commands	
68	KR 9101983 B	☐	Mfg. DRAM cell having trench-type and stack-type capacitors - is provided with mini-field oxide for connecting storage and source regions	
69	RD 309005 A	☐	Placement of random logic macro in CMPHILO bit stack - enhances efficiency of max. functions on chip when signals to macro are vertically contained in stack	
70	US 4693949 A	☐	Universal storage battery housing for e.g. automobile - has peripheral frame engaging periphery of top wall of battery and central bail overlying medial portion of top wall	
71	US 4435780 A	☐	Separate stack areas for several process - uses process control block with link field to form distributed list of processes in despatching priority order	
72	DE 3110081 A	☐	Print viewing and storage frame - has slider with plastics moulded spring tags to extract print and return it to top of stack	
73	CH 6169 7 A	☐	Extendable transportable building used as field hospital - is equipped with stacking beds stored in roof during transit, sanitary blocks and emergency operating area	
74	US 4068303 A	☐	Address translation managing system with translation pair purging - has buffer storage device swiftly translating logical address into corresponding real address	

	Document ID	U	Title	Current OR
1	US 20040047353 A1	☐	Frame transfer method and node in network, and frame transfer program	370/395.63
2	US 20040042268 A1	☐	ONE-DEVICE NON-VOLATILE RANDOM ACCESS MEMORY CELL	365/185.08
3	US 20040015927 A1	☐	Percolating hot function store/restores to colder calling functions	717/155
4	US 20040010754 A1	☐	System and method for transformation of XML documents using stylesheets	715/513
5	US 20040003377 A1	☐	Converting byte code instructions to a new instruction set	717/136
6	US 20030226022 A1	☐	Secure execution mode exceptions	713/189
7	US 20030226014 A1	☐	Trusted client utilizing security kernel under secure execution mode	713/164
8	US 20030221085 A1	☐	Implementation of thread-static data in multi-threaded computer systems	711/220
9	US 20030218632 A1	☐	Method and architecture of an event transform oriented operating environment for a personal mobile display system	345/740
10	US 20030217327 A1	☐	Compiling method with exception handling	714/798
11	US 20030212988 A1	☐	Preserving program context when adding probe routine calls for program instrumentation	717/130
12	US 20030209754 A1	☐	Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming, reading and erasing said memory structure	257/314
13	US 20030173643 A1	☐	Silicide-silicon oxide-semiconductor antifuse device and method of making	257/530
14	US 20030172293 A1	☐	System and method of foiling buffer-overflow and alien-code attacks	713/200
15	US 20030167373 A1	☐	Method and system for reducing storage requirements for program code in a communication device	711/103
16	US 20030156757 A1	☐	Image processing apparatus and method for recognizing specific pattern and recording medium having image processing program recorded thereon	382/195
17	US 20030140338 A1	☐	Method, apparatus and article for generation of debugging information	717/162

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

DATED : July 23, 1996

INVENTOR(S): Nguyen *et al.*

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below.

In column 1, at line 36 insert therein:

--Page Printer Controller Including A Single Chip Superscalar Microprocessor With Graphics Functional Units, invented by Lentz *et al.*, Application Serial Number 08/267,646 filed June 28, 1994, now U.S. Patent No. 5,394,515, which is a continuation of 07/817,813, filed January 8, 1992, which is a continuation of 07/726,929, filed July 8, 1991; and--;

in column 14, at line 12, delete "So" and insert therein --to--; and

Column 44, line 28,
in Table III, at "reserved" row, move "0110" from middle column to last column, titled "Instruction Symbol Condition Code".

Signed and Sealed this

Twenty-ninth Day of October 1996

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

	Document ID	U	Title	Current OR
18	US 20030135847 A1	☐	Uninstrumenting in-line code instrumentation via stack unwinding and cleanup	717/158
19	US 20030126590 A1	☐	System and method for dynamic data-type checking	717/154
20	US 20030120968 A1	☐	Preserving dump capability after a fault-on-fault or related type failure in a fault tolerant computer system	714/25
21	US 20030115573 A1	☐	Efficient generic code in a dynamic execution environment	717/111
22	US 20030093780 A1	☐	Annotations to executable images for improved dynamic optimization of functions	717/153
23	US 20030093545 A1	☐	Method and system for downloading data to portable electronic device	709/231
24	US 20030079202 A1	☐	Exception handling in java computing environments	717/118
25	US 20030074554 A1	☐	Broadband interface unit and associated method	713/153
26	US 20030074474 A1	☐	Data distribution center and associated method	709/246
27	US 20030074445 A1	☐	Broadband network system and associated method	709/224
28	US 20030042517 A1	☐	Field-effect transistor having a contact to one of its doping regions, and method for fabricating the transistor	257/288
29	US 20030028742 A1	☐	METHOD FOR SECURING A TYPED DATA LANGUAGE, PARTICULARLY IN AN EMBEDDED SYSTEM, AND EMBEDDED SYSTEM FOR IMPLEMENTING THE METHOD	711/172
30	US 20030023905 A1	☐	Exception handling system and method	714/34
31	US 20030012172 A1	☐	Apparatus and method for transmitting a voice frame in an all-IP-based mobile communication system	370/342
32	US 20030006450 A1	☐	Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming, reading and erasing said memory structure	257/316
33	US 20030005212 A1	☐	Method and apparatus for dynamically modifying a stored program	711/103
34	US 20020199093 A1	☐	Method and system for using internal FIFO RAM to improve system boot times	713/1

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

DATED : July 23, 1996

INVENTOR(S) : Nguyen *et al.*

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in item [56], please add the cited references:

U.S. Patent 5,003,462, dated March 26, 1991, to Blaner *et al.*

U.S. Patent 4,942,525, dated July 17, 1990, to Shintani *et al.*

U.S. Patent 4,459,657, dated July 10, 1984, to Murao

U.S. Patent 4,434,641, dated February 28, 1984, to Puhl

U.S. Patent 4,410,939, dated October 18, 1983, to Kawakami

U.S. Patent 4,296,470, dated October 20, 1981, to Fairchild *et al.*

U.S. Patent 3,346,851, dated October 31, 1976 to Thornton *et al.*

European Patent EPA 0419105 A2, dated October 9, 1990

European Patent EPA 0402856, dated December 6, 1990

European Patent EPA 0377991 A3, dated December 20, 1989

European Patent EPA 0372751 A2, dated November 22, 1989

European Patent EPA 0136179 A2, dated September 27, 1984

French Patent 2575564, dated December 27, 1985

	Document ID	U	Title	Current OR
35	US 20020194459 A1	☐	Method and apparatus for saving and restoring processor register values and allocating and deallocating stack memory	712/228
36	US 20020188931 A1	☐	Method for unwinding a program call stack	717/154
37	US 20020156991 A1	☐	Method and apparatus for 24-bit memory addressing in microcontrollers	711/219
38	US 20020138819 A1	☐	Computer programming language to describe and encapsulate a computer as a set of classes and objects	717/114
39	US 20020122205 A1	☐	Method of utilizing variable data fields with a page description language	358/1.15
40	US 20020112203 A1	☐	Fault handling in a data processing system utilizing a fault vector pointer table	714/48
41	US 20020112202 A1	☐	Fault vector pointer table	714/48
42	US 20020108103 A1	☐	Intercalling between native and non-native instruction sets	717/139
43	US 20020089681 A1	☐	Method of utilizing variable data fields with a page description language	358/1.11
44	US 20020075719 A1	☐	Low-cost three-dimensional memory array	365/130
45	US 20020072830 A1	☐	Dynamic classification of sections of software	701/1
46	US 20020059560 A1	☐	Debugging device and method	717/124
47	US 20020048501 A1	☐	Vehicle mounted large bale loading, transporting and unloading system	414/111
48	US 20020046289 A1	☐	Protocol stack for linking storage area networks over an existing LAN, MAN,or WANProtocol stack for linking storage area networks over on existing , man, or wan	709/236
49	US 20020041799 A1	☐	Vehicle mounted large bale loading, transporting and unloading system	414/111
50	US 20020035571 A1	☐	Digital patent marking method	707/104.1
51	US 20020032804 A1	☐	Heavyweight and lightweight instrumentation	719/320

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

DATED : July 23, 1996

INVENTOR(S) : Nguyen *et al.*

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

IEEE MICRO, vol. 9, no. 2, April 1989, Los Alamitos, CA, U.S., pages 26-38, Charles Melear, Motorola, Inc., The Design of the 88000 RISC Family.

PATENT ABSTRACTS OF JAPAN, vol. 010, no. 089, April 1986, $ JP,A,60 225 943 (Hitachi Seisakusho K K) 11 November 1985.

IEEE TRANSACTIONS ON COMPUTERS, vol. 37, no. 5, may 1988, New York, U.S., pages 562-573, J.E. Smith, A. R. Pleszkun, Implementing Precise Interrupts in Pipelined Processors.

ELECTRO CONFERENCE RECORD, vol. 14, 11 April 1989, Los Angeles, U.S. pages 511-519, Jelemensky, New Microcomputer Features Advanced Hardware for Real-Time Control Applications.

COMPUTER DESIGN, vol. 28, no. 9, 1 May 1989, Littleton, Massachussetts, U.S., pages 86-99, Andrews, Distinctions Blur Between DSP Solutions.

V. Popescu, M. Schultz, J. Spracklen, G. Gibson, B. Lightner & D. Isaman , The Metaflow Architecture, Metaflow Technologies, Inc., June, 1991.

R. Weiss, "Third-Generation RISC Processors", On Special Report, March 30, 1992, pp. 96-108.

	Document ID	U	Title	Current OR
52	US 20020 03271 8 A1	☐	METHOD AND APPARATUS FOR MAINTAINING TRANSLATED ROUTINE STACK IN A BINARY TRANSLATION ENVIROMENT	718/107
53	US 20020 01390 7 A1	☐	Method of preventing stack manipulation attacks during function calls	713/200
54	US 20010 05583 8 A1	☐	Nonvolatile memory on SOI and compound semiconductor substrates and method of fabrication	438/129
55	US 20010 00759 2 A1	☐	Biometric combination lock	382/116
56	US 67082 73 B1	☐	Apparatus and method for implementing IPSEC transforms within an integrated circuit	713/189
57	US 67048 71 B1	☐	Cryptographic co-processor	713/192
58	US 66979 59 B2	☐	Fault handling in a data processing system utilizing a fault vector pointer table	714/10
59	US 66955 60 B2	☐	Vehicle mounted large bale loading, transporting and unloading system	414/111
60	US 66912 19 B2	☐	Method and apparatus for 24-bit memory addressing in microcontrollers	711/219
61	US 66878 45 B2	☐	Fault vector pointer table	714/2
62	US 66870 16 B2	☐	Method of utilizing variable data fields with a page description language	358/1.11
63	US 66657 93 B1	☐	Method and apparatus for managing access to out-of-frame Registers	712/228
64	US 66434 00 B1	☐	Image processing apparatus and method for recognizing specific pattern and recording medium having image processing program recorded thereon	382/195
65	US 66314 60 B1	☐	Advanced load address table entry invalidation based on register address wraparound	712/217
66	US 66291 23 B1	☐	Interception of unit creation requests by an automatic distributed partitioning system	718/106
67	US 65981 51 B1	☐	Stack Pointer Management	712/228
68	US 65801 20 B2	☐	Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming, reading and erasing said memory structure	257/315
69	US 65500 58 B1	☐	Stack clearing device and method	717/158
70	US 65499 59 B1	☐	Detecting modification to computer memory by a DMA device	710/22
71	US 65359 03 B2	☐	Method and apparatus for maintaining translated routine stack in a binary translation environment	718/100
72	US 65158 88 B2	☐	Low cost three-dimensional memory array	365/130

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

DATED : July 23, 1996

INVENTOR(S) : Nguyen *et al.*

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Johnson, Superscalar Microprocessor Design, Prentice-Hall, Inc., 1991, (in its entirety).

J. Hennessy & D. Patterson, Computer Architecture A Quantitative Approach, Morgan Kaufmann Publishers, Inc., 1990, (in its entirety).

Signed and Sealed this

Nineteenth Day of October, 1999

Attest:

Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks

	Document ID	U	Title	Current OR
73	US 6502237 B1	☐	Method and apparatus for performing binary translation method and apparatus for performing binary translation	717/136
74	US 6502181 B1	☐	Method and apparatus for an enhanced processor	712/32
75	US 6499137 B1	☐	Reversible load-time dynamic linking	717/164
76	US 6490721 B1	☐	Software debugging method and apparatus	717/130
77	US 6483911 B1	☐	Methods and apparatus for providing external access to executable call flows of a network application	379/201.03
78	US 6481006 B1	☐	Method and apparatus for efficient invocation of Java methods from native codes	717/139
79	US 6467016 B1	☐	Apparatus to record digital data on non-volatile memory card for recording in units of blocks of digital data and method thereof	711/103
80	US 6463538 B1	☐	Method of software protection using a random code generator	713/190
81	US 6397379 B1	☐	Recording in a program execution profile references to a memory-mapped active device	717/140
82	US 6389540 B1	☐	Stack based access control using code and executor identifiers	713/200
83	US 6381735 B1	☐	Dynamic classification of sections of software	717/158
84	US 6381628 B1	☐	Summarized application profiling and quick network profiling	709/201
85	US 6381028 B1	☐	Method of utilizing variable data fields with a page description language	358/1.11
86	US 6378061 B1	☐	Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit	712/200
87	US 6376312 B1	☐	Formation of non-volatile memory device comprised of an array of vertical field effect transistor structures	438/268
88	US 6373967 B2	☐	Biometric combination lock	382/115
89	US 6363521 B1	☐	Process for processing programs, process for detecting depth of frame associated with specified method, detection method, and computer	717/128
90	US 6363474 B1	☐	Process switching register replication in a data processing system	712/202
91	US 6345383 B1	☐	Debugging support device and debugging support method	717/124
92	US 6328520 B1	☐	Vehicle mounted large bale loading, transporting and unloading system	414/111
93	US 6317869 B1	☐	Method of run-time tracking of object references in Java programs	717/132
94	US 6314513 B1	☐	Method and apparatus for transferring data between a register stack and a memory resource	712/228
95	US 6301699 B1	☐	Method for detecting buffer overflow for computer security	717/131

	Document ID	U	Title	Current OR
96	US 6301650 B1	☐	Control unit and data processing system	712/35
97	US 6293712 B1	☐	Method and apparatus for constructing a stack unwind data structure	717/155
98	US 6282700 B1	☐	Mechanism for maintaining revisions of objects in flash memory	717/170
99	US 6272613 B1	☐	Method and system for accessing storage area of a digital data processing machine in both the physical and virtual addressing modes	711/204
100	US 6263491 B1	☐	Heavyweight and lightweight instrumentation	717/130
101	US 6263401 B1	☐	Method and apparatus for transferring data between a register stack and a memory resource	711/109
102	US 6247170 B1	☐	Method and data processing system for providing subroutine level instrumentation statistics	717/131
103	US 6230312 B1	☐	Automatic detection of per-unit location constraints	717/108
104	US 6229906 B1	☐	Biometric sequence codes	382/116
105	US 6226789 B1	☐	Method and apparatus for data flow analysis	717/138
106	US 6220811 B1	☐	Apparatus and method for handling and transporting bales	414/555
107	US 6219666 B1	☐	Autonomous transactions in a database system	707/8
108	US 6219072 B1	☐	Microcomputer with a built in character display circuit and visual display unit using such a microcomputer	345/531
109	US 6202176 B1	☐	Method of monitoring the correct execution of software programs	714/38
110	US 6199156 B1	☐	System for explicitly referencing a register for its current content when performing processor context switch	712/228
111	US 6199095 B1	☐	System and method for achieving object method transparency in a multi-code execution environment	718/107
112	US 6170043 B1	☐	Method for controlling an optic disk	711/158
113	US 6151660 A	☐	Information recording/reproducing apparatus having segmented cache memory	711/129
114	US 6151569 A	☐	Automated sequence of machine-performed attempts to unfreeze an apparently frozen application program	703/22
115	US 6138272 A	☐	GDMO translator, method of GDMO translation, and recording medium containing program for GDMO translator	717/142
116	US 6138238 A	☐	Stack-based access control using code and executor identifiers	713/200
117	US 6134655 A	☐	Method and apparatus for initializing a microprocessor to insure fault-free operation	713/1
118	US 6119206 A	☐	Design of tags for lookup of non-volatile registers	711/147

	Document ID	U	Title	Current OR
119	US 6111522 A	☐	Multiple electronic purse parking meter	340/932.2
120	US 6101580 A	☐	Apparatus and method for assisting exact garbage collection by using a stack cache of tag bits	711/132
121	US 6093216 A	☐	Method of run-time tracking of object references in Java programs	717/128
122	US 6091897 A	☐	Fast translation and execution of a computer program on a non-native architecture by use of background translator	717/138
123	US 6081665 A	☐	Method for efficient soft real-time execution of portable byte code computer programs	717/116
124	US 6070057 A	☐	System and method for improving reliability and performance of wireless communication systems using message pooling	455/67.13
125	US 6055414 A	☐	System and method for improving reliability and performance of wireless communication systems using message pooling	455/67.13
126	US 6038611 A	☐	Method for implementing a user-to-network (UNI) application programming interface (API)	719/328
127	US 6014674 A	☐	Method for maintaining log compatibility in database systems	707/202
128	US 6014515 A	☐	Enhanced stack unwind facility	717/129
129	US 6009517 A	☐	Mixed execution stack and exception handling	712/245
130	US 6009258 A	☐	Methods and devices for unwinding stack of frozen program and for restarting the program from unwound state	703/22
131	US 6000028 A	☐	Means and apparatus for maintaining condition codes in an unevaluated state	712/226
132	US 5983018 A	☐	Debug interrupt-handling microcomputer	717/127
133	US 5982294 A	☐	Paging receiver which performs data communication protocol analysis through execution of control program	340/7.44
134	US 5956629 A	☐	Method and apparatus for transmitter identification and selection for mobile information signal services	455/166.2
135	US 5953529 A	☐	Data processor with a debug device and a stack area control unit and corresponding data processing method	717/135
136	US 5950003 A	☐	Profile instrumentation method and profile data collection method	717/130
137	US 5937186 A	☐	Asynchronous interrupt safing of prologue portions of computer programs	712/244
138	US 5937153 A	☐	Method of utilizing variable data fields with a page description language	358/1.17
139	US 5933515 A	☐	User identification through sequential input of fingerprints	382/124
140	US 5930807 A	☐	Apparatus and method for fast filtering read and write barrier operations in garbage collection system	707/206
141	US 5930509 A	☐	Method and apparatus for performing binary translation	717/159

	Document ID	U	Title	Current OR
142	US 5923883 A	☐	Optimization apparatus which removes transfer instructions by a global analysis of equivalence relations	717/156
143	US 5918037 A	☐	Generating tests for an extended finite state machine using different coverage levels for different submodels	716/2
144	US 5915266 A	☐	Processor core which provides a linear extension of an addressable memory space	711/211
145	US 5911060 A	☐	Computer method and apparatus for unfreezing an apparently frozen application program being executed under control of an operating system	718/100
146	US 5909580 A	☐	Development system and methods with direct compiler support for detecting invalid use and management of resources and memory at runtime	717/141
147	US 5909579 A	☐	Method and apparatus for encoding and decoding delta encoded information to locate live pointers in program data stacks	717/131
148	US 5907709 A	☐	Development system with methods for detecting invalid use and management of resources and memory at runtime	717/141
149	US 5899985 A	☐	Inference method and inference system	706/45
150	US 5893121 A	☐	System and method for swapping blocks of tagged stack entries between a tagged stack cache and an untagged main memory storage	707/206
151	US 5882163 A	☐	Front-end big bale loader	414/111
152	US 5857096 A	☐	Microarchitecture for implementing an instruction to clear the tags of a stack reference register file	712/229
153	US 5848423 A	☐	Garbage collection system and method for locating root set pointers in method activation records	707/206
154	US 5848295 A	☐	System for allocating common memory in cache such that data is maintained when exiting first programming structure and entering second programming structure	710/7
155	US 5842017 A	☐	Method and apparatus for forming a translation unit	717/158
156	US 5813033 A	☐	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
157	US 5807053 A	☐	Multiple hay bale transporter and loader	414/24.5
158	US 5805874 A	☐	Method and apparatus for performing a vector skip instruction in a data processor	712/222
159	US 5802373 A	☐	Method for providing a pipeline interpreter for a variable length instruction set	717/139
160	US 5802267 A	☐	Method for checkpointing in computer system under distributed processing environment	714/15
161	US 5787474 A	☐	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138
162	US 5761491 A	☐	Data processing system and method for storing and restoring a stack pointer	712/244
163	US 5754805 A	☐	Instruction in a data processing system utilizing extension bits and method therefor	712/200
164	US 5754759 A	☐	Testing and monitoring of programmed devices	714/37

	Document ID	U	Title	Current OR
165	US 5752074 A	☐	Data processing system and method thereof	712/29
166	US 5751988 A	☐	Microcomputer with memory bank configuration and register bank configuration	711/5
167	US 5742786 A	☐	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	711/217
168	US 5740443 A	☐	Call-site specific selective automatic inlining	717/133
169	US 5737586 A	☐	Data processing system and method thereof	712/236
170	US 5734879 A	☐	Saturation instruction in a data processor	712/221
171	US 5732272 A	☐	Subroutine execution time tracer	717/128
172	US 5729748 A	☐	Call template builder and method	717/137
173	US 5729665 A	☐	Method of utilizing variable data fields with a page description language	358/1.18
174	US 5717947 A	☐	Data processing system and method thereof	712/3
175	US 5706488 A	☐	Data processing system and method thereof	712/223
176	US 5675827 A	☐	Information processing system, a processor, and an information processing method for the performing of an arithmetic operation of numeric information	715/538
177	US 5666510 A	☐	Data processing device having an expandable address space	711/220
178	US 5664134 A	☐	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	712/245
179	US 5664060 A	☐	Message management methods and apparatus	704/270
180	US 5647716 A	☐	Tined, front-end big bale loader	414/111
181	US 5644709 A	☐	Method for detecting computer memory access errors	714/53
182	US 5640541 A	☐	Adapter for interfacing a SCSI bus with an IBM system/360/370 I/O interface channel and information system including same	703/26
183	US 5638517 A	☐	Method and apparatus for transmitting a message from a computer system over a network adapter to the network by performing format conversion and memory verification	709/246
184	US 5636362 A	☐	Programmable high watermark in stack frame cache using second region as a storage if first region is full and an event having a predetermined minimum priority	711/129
185	US 5618146 A	☐	Hay roll transporter	414/24.5
186	US 5617532 A	☐	Information processing apparatus and data back-up/restore system for the information processing apparatus	714/36
187	US 5600846 A	☐	Data processing system and method thereof	712/5

	Document ID	U	Title	Current OR
188	US 5598571 A	☐	Data processor for conditionally modifying extension bits in response to data processing instruction execution	712/9
189	US 5586293 A	☐	Real time cache implemented by on-chip memory having standard and cache operating modes	711/118
190	US 5572689 A	☐	Data processing system and method thereof	712/200
191	US 5566308 A	☐	Processor core which provides a linear extension of an addressable memory space	711/2
192	US 5563828 A	☐	Method and apparatus for searching for data in multi-bit flash EEPROM memory arrays	365/185.33
193	US 5559973 A	☐	Data processing system and method thereof	712/241
194	US 5551039 A	☐	Compiling a source code vector instruction by generating a subgrid loop for iteratively processing array elements by plural processing elements	717/150
195	US 5548768 A	☐	Data processing system and method thereof	712/200
196	US 5541886 A	☐	Method and apparatus for storing control information in multi-bit non-volatile memory arrays	365/185.03
197	US 5537562 A	☐	Data processing system and method thereof	712/234
198	US 5519517 A	☐	Method and apparatus for holographically recording and reproducing images in a sequential manner	359/22
199	US 5504922 A	☐	Virtual machine with hardware display controllers for base and target machines	703/25
200	US 5475693 A	☐	Error management processes for flash EEPROM memory arrays	714/710

	L #	Hits	Search Text	DBs
1	L1	28267	stack near10 (frame area region space)	USPAT; US-PGPUB
2	L3	12095	stack near10 (frame area region space)	EPO; JPO; DERWENT; IBM_TDB
3	L4	74	(bit field tag flag cod$3 encod$3) near10 (sav$3 stor$3) near15 3	EPO; JPO; DERWENT; IBM_TDB
4	L2	285	(bit field tag flag cod$3 encod$3) near10 (sav$3 stor$3) near15 1	USPAT; US-PGPUB
5	L15	9164	(bit field tag flag) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
6	L18	29308	(bit field tag flag) near10 instruction	USPAT; US-PGPUB
7	L17	34	(register near20 stack) near99 15	EPO; JPO; DERWENT; IBM_TDB
8	L23	443	(register near20 stack) near99 (18 near20 register)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 2000284967 A	☐	MICROCOMPUTER	
2	JP 10021117 A	☒	DEVICE AND METHOD FOR CONTROLLING PROGRAM EXECUTION	
3	JP 06095958 A	☒	DATA TABLE SYSTEM	
4	JP 05334100 A	☒	MICROPROCESSOR	
5	JP 05061670 A	☒	INTERRUPTION PROCESSING METHOD BASED UPON FLUG CONTROL	
6	JP 04052962 A	☒	ACCESS MASK CONTROL SYSTEM	
7	JP 04040530 A	☒	REAL TIME PROCESSOR	
8	JP 03083737 A	☒	FEEDER TRANSMISSION OF PAPER FACSIMILE MACHINE	
9	JP 03036629 A	☒	INFORMATION PROCESSOR	
10	JP 02250174 A	☒	VECTOR PROCESSING DEVICE	
11	JP 62145326 A	☒	MICROPROGRAM CONTROL CIRCUIT	
12	JP 62044836 A	☒	MICROADDRESS STACK CONTROL SYSTEM	
13	JP 62025333 A	☒	MICROCOMPUTER	
14	JP 61289430 A	☒	MICROCOMPUTER	
15	JP 61188628 A	☒	INSTRUCTION PROCESSING AND CONTROLLER SYSTEM IN INFORMATION PROCESSOR	
16	JP 61148533 A	☒	INFORMATION PROCESSOR	
17	JP 61101838 A	☒	INSTRUCTION DECODE SYSTEM	
18	JP 61082244 A	☒	INTER-TASK DATA TRANSMITTING AND RECEIVING SYSTEM	
19	JP 61032148 A	☒	DESIGNATION INSTRUCTION TRACE SYSTEM	
20	JP 55115155 A	☒	ONE CHIP MULTI-MICROCOMPUTER	
21	EP 363174 A2	☒	Branch on bit processing.	
22	NN86044737	☒	Indirect Program Access for a Signal Processor	

	Document ID	U	Title	Current OR
23	US 20020 19445 9 A	☒	Instruction encoding method for data processing system, involves storing register value as argument or static value in stack memory location set by calling or called program, based on encoded field	
24	US 59789 01 A	☒	Floating point and multimedia unit with instruction reclassifier for superscalar processor	
25	EP 93128 6 A	☒	Stack oriented architecture for microprocessor	
26	US 58125 62 A	☒	VLSIC operating method for testing and debugging purpose - involves shifting control values which includes stop clock flag request bit into control register while system clock is provided to function block	
27	US 57908 54 A	☒	Vector data processor for fuzzy logic - involves retrieving specific value from stack and stored as current Vt bit mask, if conditional statement is false	
28	EP 36388 9 A	☒	Vector processor vector data prepn. - has buffer in memory controller storing vector data in response to decoder request signal	
29	EP 36317 4 A	☒	Detection branch on bit unit for data processing system - provides branching on variable branch condition or status parameters selectable by program instructions	
30	EP 35208 2 A	☒	Operating memory stack in high-speed CPU - unconditionally writing from write bus to register of pointed to stack, an copying contents of register to read bus	
31	EP 18479 1 A	☒	Information processor carrying out vector calculation - has state indication unit producing flags representing internal states of instruction processing unit	
32	EP 12612 4 A	☒	Pipelined micro-controller with multiple store access for clock cycle - has microinstructions comprising jump address, control and instruction fields to handle nested subroutines	
33	EP 10667 1 A	☒	Pre-etching instructions for multi-staged or pipe-lined CPU - using transfer and indirect prediction table predicting target address of transfer and indirect instructions based on history of execution	
34	EP 74479 A	☐	Data processor with architecture - permits inter-segment programme calls with associated selective allocation of data segments of varying length	

	Document ID	U	Title	Current OR
1	US 20040059895 A1	☐	Microprocessor circuit for portable data carriers and method for operating the circuit	712/223
2	US 20040042490 A1	☒	State record processing	370/469
3	US 20040015678 A1	☒	Microprocessor for executing byte compiled Java code	712/202
4	US 20040006687 A1	☒	Processor and instruction control method	712/220
5	US 20040006685 A1	☒	Processor and instruction control method	712/218
6	US 20030231634 A1	☒	Table driven programming system for a services processor	370/395.32
7	US 20030217199 A1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/1
8	US 20030212878 A1	☒	Scaleable microprocessor architecture	712/23
9	US 20030200419 A1	☒	Non-copy shared stack and register file device and dual language processor structure using the same	712/202
10	US 20030193949 A1	☒	Packet processing device	370/392
11	US 20030191929 A1	☒	Microinstruction pointer stack in a processor	712/245
12	US 20030188128 A1	☒	Executing stack-based instructions within a data processing apparatus arranged to apply operations to data items stored in registers	712/202
13	US 20030177342 A1	☒	Processor with register dirty bits and special save multiple/return instructions	712/228
14	US 20030177337 A1	☒	Computer system	712/202
15	US 20030152078 A1	☒	Services processor having a packet editing unit	370/389
16	US 20030135844 A1	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
17	US 20030135719 A1	☒	Method and system using hardware assistance for tracing instruction disposition information	712/227

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18	US 20030120903 A1	☒	Load/move and duplicate instructions for a processor	712/221
19	US 20030105793 A1	☒	Long instruction word controlling plural independent processor operations	708/625
20	US 20030023905 A1	☒	Exception handling system and method	714/34
21	US 20030018681 A1	☒	System and method for recovering applications	718/102
22	US 20020194459 A1	☒	Method and apparatus for saving and restoring processor register values and allocating and deallocating stack memory	712/228
23	US 20020179719 A1	☒	Selective access to multiple registers having a common name	235/492
24	US 20020157000 A1	☒	Software hint to improve the branch target prediction accuracy	712/239
25	US 20020144091 A1	☒	Method and apparatus for dynamic register management in a processor	712/217
26	US 20020138715 A1	☒	Microprocessor executing data transfer between memory and register and data transfer between registers in response to single push/pop instruction	712/225
27	US 20020138712 A1	☒	Data processing device with instruction translator and memory interface device	712/205
28	US 20020129225 A1	☒	Processing device for executing virtual machine instructions	712/227
29	US 20020103991 A1	☒	Multi-cycle instructions	712/219
30	US 20020097667 A1	☒	Cyclic buffer for infrared	370/205
31	US 20020066004 A1	☒	Storing stack operands in registers	712/209
32	US 20020054612 A1	☒	Integrated circuit configurations and methods for providing functions for public telephones	370/535
33	US 20020046372 A1	☒	SEQUENCE CONTROL CIRCUIT	714/718
34	US 20020042909 A1	☒	Retargetable compiling system and method	717/149

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35	US 20010044866 A1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/305
36	US 20010032296 A1	☒	Data processor	711/128
37	US 20010010072 A1	☒	Instruction translator translating non-native instructions for a processor into native instructions therefor, instruction memory with such translator, and data processing apparatus using them	712/209
38	US 6691306 B1	☒	Use of limited program space of general purpose processor for unlimited sequence of translated instructions	717/139
39	US 6666383 B2	☒	Selective access to multiple registers having a common name	235/492
40	US 6665793 B1	☒	Method and apparatus for managing access to out-of-frame Registers	712/228
41	US 6658471 B1	☒	Method and system for zero overhead software performance measurement instrumentation	709/224
42	US 6654934 B1	☒	Programmable event engine	716/4
43	US 6651159 B1	☒	Floating point register stack management for CISC	712/209
44	US 6633974 B1	☒	Apparatus and method for controlling link stack corruption during speculative instruction branching using multiple stacks	712/237
45	US 6615300 B1	☒	Fast look-up of indirect branch destination in a dynamic translation system	710/100
46	US 6604190 B1	☒	Data address prediction structure and a method for operating the same	712/207
47	US 6598149 B1	☒	Performance enhancement for code transitions of floating point and packed data modes	712/222
48	US 6598148 B1	☒	High performance microprocessor having variable speed system clock	712/32
49	US 6587910 B2	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/306
50	US 6580456 B1	☒	Programmable timing generator	348/312
51	US 6574728 B1	☒	Condition code stack architecture systems and methods	712/234
52	US 6567933 B1	☒	Emulation suspension mode with stop mode extension	714/31
53	US 6564339 B1	☒	Emulation suspension mode handling multiple stops and starts	714/30
54	US 6560692 B1	☒	Data processing circuit, microcomputer, and electronic equipment	712/23
55	US 6557116 B1	☒	Emulation suspension mode with frame controlled resource access	714/28
56	US 6553513 B1	☒	Emulation suspend mode with differing response to differing classes of interrupts	714/28

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57	US 6526503 B1	☒	Apparatus and method for accessing a memory device during speculative instruction branching	712/242
58	US 6519696 B1	☒	Paired register exchange using renaming register map	712/222
59	US 6507904 B1	☒	Executing isolated mode instructions in a secure system running in privilege rings	712/229
60	US 6477702 B1	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
61	US 6449709 B1	☒	Fast stack save and restore system and method	712/202
62	US 6442673 B1	☒	Update forwarding cache for address mode	712/202
63	US 6430670 B1	☒	Apparatus and method for a virtual hashed page table	711/216
64	US 6421773 B1	☒	Sequence control circuit	712/234
65	US 6408985 B1	☒	Motor driven lubricator	184/37
66	US 6408320 B1	☒	Instruction set architecture with versatile adder carry control	708/518
67	US 6405305 B1	☒	Rapid execution of floating point load control word instructions	712/222
68	US 6393549 B1	☒	Instruction alignment unit for routing variable byte-length instructions	712/204
69	US 6370558 B1	☒	Long instruction word controlling plural independent processor operations	708/603
70	US 6367005 B1	☒	System and method for synchronizing a register stack engine (RSE) and backing memory image with a processor's execution of instructions during a state saving context switch	712/228
71	US 6349377 B1	☒	Processing device for executing virtual machine instructions that includes instruction refeeding means	712/22
72	US 6338134 B1	☒	Method and system in a superscalar data processing system for the efficient processing of an instruction by moving only pointers to data	712/217
73	US 6332187 B1	☒	Cumulative lookahead to eliminate chained dependencies	712/23
74	US 6314513 B1	☒	Method and apparatus for transferring data between a register stack and a memory resource	712/228
75	US 6301650 B1	☒	Control unit and data processing system	712/35
76	US 6298434 B1	☒	Data processing device for processing virtual machine instructions	712/209
77	US 6292935 B1	☒	Method for fast translation of java byte codes into efficient native processor code	717/148
78	US 6289444 B1	☒	Media storage device with embedded data filter for dynamically processing data during read and write operations	710/5
79	US 6289417 B1	☒	Operand supply to an execution unit	711/131

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80	US 6272596 B1	☒	Data processor	711/128
81	US 6269436 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
82	US 6266727 B1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/105
83	US 6256725 B1	☒	Shared datapath processor utilizing stack-based and register-based storage spaces	712/200
84	US 6256721 B1	☒	Register renaming in which moves are accomplished by swapping tags	712/23
85	US 6247171 B1	☒	Bytecode program interpreter apparatus and method with pre-verification of a data type restrictions and object initialization	717/126
86	US 6240503 B1	☒	Cumulative lookahead to eliminate chained dependencies	712/23
87	US 6240437 B1	☒	Long instruction word controlling plural independent processor operations	708/524
88	US 6237083 B1	☒	Microprocessor including multiple register files mapped to the same logical storage and inhibiting sychronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
89	US 6233672 B1	☒	Piping rounding mode bits with floating point instructions to eliminate serialization	712/222
90	US 6233637 B1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/311
91	US 6219783 B1	☒	Method and apparatus for executing a flush RS instruction to synchronize a register stack with instructions executed by a processor	712/228
92	US 6219688 B1	☒	Method, apparatus and system for sum of plural absolute differences	708/709
93	US 6216214 B1	☒	Apparatus and method for a virtual hashed page table	711/207
94	US 6209082 B1	☒	Apparatus and method for optimizing execution of push all/pop all instructions	712/225
95	US 6205541 B1	☒	System and method using selection logic units to define stack orders	712/217
96	US 6205223 B1	☒	Input data format autodetection systems and methods	380/42
97	US 6189068 B1	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
98	US 6185629 B1	☒	Data transfer controller employing differing memory interface protocols dependent upon external input at predetermined time	710/10
99	US 6173394 B1	☒	Instruction having bit field designating status bits protected from modification corresponding to arithmetic logic unit result	712/226
100	US 6173305 B1	☒	Division by iteration employing subtraction and conditional source selection of a prior difference or a left shifted remainder	708/650
101	US 6134573 A	☒	Apparatus and method for absolute floating point register addressing	708/510

	Document ID	U	Title	Current OR
102	US 61167 68 A	☒	Three input arithmetic logic unit with barrel rotator	708/236
103	US 61157 77 A	☒	LOADRS instruction and asynchronous context switch	710/260
104	US 61122 96 A	☒	Floating point stack manipulation using a register map and speculative top of stack values	712/222
105	US 61122 92 A	☒	Code sequence for asynchronous backing store switch utilizing both the cover and LOADRS instructions	712/200
106	US 61120 18 A	☒	Apparatus for exchanging two stack registers	712/202
107	US 60981 67 A	☒	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
108	US 60981 63 A	☒	Three input arithmetic logic unit with shifter	712/20
109	US 60947 16 A	☒	Register renaming in which moves are accomplished by swapping rename tags	712/23
110	US 60817 83 A	☒	Dual processor digital audio decoder with shared memory data transfer and task partitioning for decompressing compressed audio data, and systems and methods using the same	704/500
111	US 60790 08 A	☒	Multiple thread multiple data predictive coded parallel processing system and method	712/11
112	US 60790 06 A	☒	Stride-based data address prediction structure	711/213
113	US 60702 52 A	☒	Method and apparatus for interactive built-in-self-testing with user-programmable test patterns	714/30
114	US 60676 13 A	☒	Rotation register for orthogonal data transformation	712/32
115	US 60651 14 A	☒	Cover instruction and asynchronous backing store switch	712/228
116	US 60617 85 A	☒	Data processing system having an apparatus for out-of-order register operations and method therefor	712/236
117	US 60617 11 A	☒	Efficient context saving and restoring in a multi-tasking computing system environment	718/108
118	US 60584 73 A	☒	Memory store from a register pair conditional upon a selected status bit	712/225
119	US 60584 67 A	☒	Standard cell, 4-cycle, 8-bit microcontroller	712/32
120	US 60556 19 A	☒	Circuits, system, and methods for processing multiple data streams	712/36
121	US 60321 70 A	☒	Long instruction word controlling plural independent processor operations	708/620
122	US 60264 84 A	☒	Data processing apparatus, system and method for if, then, else operation using write priority	712/226
123	US 60187 98 A	☒	Floating point unit using a central window for storing instructions capable of executing multiple instructions in a single clock cycle	712/220
124	US 60165 44 A	☒	Apparatus and method for tracking changes in address size and for different size retranslate second instruction with an indicator from address size	712/234

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125	US 6016538 A	☒	Method, apparatus and system forming the sum of data in plural equal sections of a single data word	712/32
126	US 6014734 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
127	US 6012128 A	☒	Microcontroller having a page address mode	711/163
128	US 6009511 A	☒	Apparatus and method for tagging floating point operands and results for rapid detection of special floating point numbers	712/222
129	US 6009509 A	☒	Method and system for the temporary designation and utilization of a plurality of physical registers as a stack	712/202
130	US 6006324 A	☒	High performance superscalar alignment unit	712/204
131	US 6003134 A	☒	Secure open smart card architecture	713/200
132	US 6003128 A	☒	Number of pipeline stages and loop length related counter differential based end-loop prediction	712/241
133	US 5999731 A	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
134	US 5995748 A	☒	Three input arithmetic logic unit with shifter and/or mask generator	712/221
135	US 5995747 A	☒	Three input arithmetic logic unit capable of performing all possible three operand boolean operations with shifter and/or mask generator	712/221
136	US 5987596 A	☒	Register rename stack for a microprocessor	712/217
137	US 5987561 A	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
138	US 5983328 A	☒	Data processing device with time-multiplexed memory bus	711/157
139	US 5983307 A	☒	Electrical circuit for exchanging data between a microprocessor and a memory and computer comprising a circuit of this type	710/310
140	US 5978907 A	☒	Delayed update register for an array	712/239
141	US 5978901 A	☒	Floating point and multimedia unit with data type reclassification capability	712/222
142	US 5978825 A	☒	Zero detection circuitry and methods	708/525
143	US 5974539 A	☒	Three input arithmetic logic unit with shifter and mask generator	712/221
144	US 5974533 A	☒	Data processor	712/211
145	US 5974432 A	☒	On-the-fly one-hot encoding of leading zero count	708/205
146	US 5968169 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
147	US 5961635 A	☒	Three input arithmetic logic unit with barrel rotator and mask generator	712/221

	Document ID	U	Title	Current OR
148	US 5960193 A	☒	Apparatus and system for sum of plural absolute differences	712/221
149	US 5949996 A	☒	Processor having a variable number of stages in a pipeline	712/244
150	US 5944812 A	☒	Register rename stack for a microprocessor	712/23
151	US 5944801 A	☒	Isochronous buffers for MMx-equipped microprocessors	710/29
152	US 5940311 A	☒	Immediate floating-point operand reformatting in a microprocessor	708/204
153	US 5935239 A	☒	Parallel mask decoder and method for generating said mask	712/224
154	US 5933618 A	☒	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
155	US 5931943 A	☒	Floating point NaN comparison	712/222
156	US 5930492 A	☒	Rapid pipeline control using a control word and a steering word	712/216
157	US 5922068 A	☒	Information processing system and information processing method for executing instructions in parallel	712/215
158	US 5913924 A	☒	Use of a stored signal to switch between memory banks	711/212
159	US 5913048 A	☒	Dispatching instructions in a processor supporting out-of-order execution	712/215
160	US 5913047 A	☒	Pairing floating point exchange instruction with another floating point instruction to reduce dispatch latency	712/213
161	US 5909567 A	☒	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
162	US 5907864 A	☒	Data processing device with time-multiplexed memory bus	711/169
163	US 5895497 A	☒	Microprocessor with pipelining, memory size evaluation, micro-op code and tags	711/169
164	US 5892936 A	☒	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
165	US 5887185 A	☒	Interface for coupling a floating point unit to a reorder buffer	712/23
166	US 5887161 A	☒	Issuing instructions in a processor supporting out-of-order execution	712/244
167	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
168	US 5884062 A	☒	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	712/218
169	US 5881305 A	☒	Register rename stack for a microprocessor	712/23
170	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242

	Document ID	U	Title	Current OR
171	US 5878255 A	☒	Update unit for providing a delayed update to a branch prediction array	712/240
172	US 5875324 A	☒	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
173	US 5875315 A	☒	Parallel and scalable instruction scanning unit	712/204
174	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
175	US 5860104 A	☒	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137
176	US 5859991 A	☒	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
177	US 5857096 A	☒	Microarchitecture for implementing an instruction to clear the tags of a stack reference register file	712/229
178	US 5854921 A	☒	Stride-based data address prediction structure	712/239
179	US 5852726 A	☒	Method and apparatus for executing two types of instructions that specify registers of a shared logical register file in a stack and a non-stack referenced manner	712/200
180	US 5850543 A	☒	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238
181	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
182	US 5835973 A	☒	Instruction processing unit capable of efficiently accessing the entire address space of an external memory	711/220
183	US 5835967 A	☒	Adjusting prefetch size based on source of prefetch address	711/213
184	US 5835951 A	☒	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
185	US 5832297 A	☒	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
186	US 5832249 A	☒	High performance superscalar alignment unit	712/204
187	US 5826071 A	☒	Parallel mask decoder and method for generating said mask	712/224
188	US 5826057 A	☒	Method for managing virtual address space at improved space utilization efficiency	703/24
189	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
190	US 5822559 A	☒	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
191	US 5822558 A	☒	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
192	US 5819059 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213

	Document ID	U	Title	Current OR
193	US 5819057 A	☒	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
194	US 5813033 A	☒	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
195	US 5812813 A	☒	Apparatus and method for of register changes during execution of a micro instruction tracking sequence	712/218
196	US 5812562 A	☒	Low cost emulation scheme implemented via clock control using JTAG controller in a scan environment	714/726
197	US 5809274 A	☒	Purge control for ON-chip cache memory	712/210
198	US 5805913 A	☒	Arithmetic logic unit with conditional register source selection	712/209
199	US 5790854 A	☒	Efficient stack utilization for compiling and executing nested if-else constructs in a vector data processing system	717/150
200	US 5787474 A	☒	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138